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MARK M. TAKAHASHI
GRAY CARY WARE & FREIDENRICH, LLP
4365 EXECUTIVE DRIVE, SUITE 1100
SAN DIEGO, CA 92121-2133

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/772,591	LEE ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *29 January 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been considered.

Drawings

2. The drawings are objected to because in Figure 1 and Figure 3 have elements labeled "RC". It is unclear from the specification what "RC" abbreviates. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 2, elements 202A, 202B, and 202C. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Page 4, line 20 "CONTROL1" and Page 4, line 22 "CONTROL2". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 8 objected to because of the following informalities: The claim ends with "and" indicating there are more limitations. However, there are no limitations following the MIMD mode. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being taught by Wilkinson et al., U.S. Patent Number 5,282,894 (herein referred to as Wilkinson).

8. Referring to claim 1, Wilkinson has taught an apparatus for programming an MxN array of reconfigurable processor cells, each cell being operative according to a context instruction (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2), comprising:

a. An execution mode signal generator, connected to each cell in the array and having an execution mode signal for controlling an execution mode of each cell (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2). In regards to Wilkinson, the execution mode is dictated by the instruction to be processed by the elements.

b. An enable register connected to the array and providing an enable signal to each cell in the array for controlling delivery of a next context instruction to each enabled cell based on the execution mode (Wilkinson Abstract; column 8, lines

52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2). In regards to Wilkinson, the enable register is inherent since the signals which indicate which processing elements are not dozing must be stored somewhere.

9. Referring to claim 2, Wilkinson has taught wherein the enable register further comprises:

a. A row enable register connected to each row of the array and having an M-bit row enable signal for controlling an active state of each cell in a row (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2); and

b. A column enable register connected to each column of the array and having an N-bit column enable signal for controlling an active state of each cell in a column (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2).

10. Referring to claim 3, Wilkinson has taught a context memory, responsive to the enable signal and the execution mode signal, for delivering the next context instruction to each active cell in the array (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2).

11. Referring to claim 4, Wilkinson has taught wherein a default state of each cell in the array is an enabled state (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2).

12. Referring to claim 5, Wilkinson has taught an enable signal loader connected to the enable register and responsive to an address signal for selecting a subset of cells in the array for enabling (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2). In regards to Wilkinson, the pickets determine which group it is in according to its properties, while the signal which indicates which group is being enabled is activated, and fetches data from the address provided accordingly.

13. Referring to claim 6, Wilkinson has taught wherein the context memory includes a context register connected to each cell in the array, wherein the context register is connected to the enable signal (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2). In regards to Wilkinson, the memory which provides the context, or instruction, to be executed functions the same as the context register.

14. Referring to claim 7, Wilkinson has taught a SMID/MIMD system for processing data, comprising:

a. An M row x N column array of independently enabled processing cells, wherein each cell includes a context register for storing a context instruction which controls an operation unit of the cell (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2);

b. An enable register having a row enable register for providing a row enable signal to each row in the array, and a column enable register for providing a column enable signal to each column in the array (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2). In regards to Wilkinson, the enable register is inherent since the signals which indicate which processing elements are not dozing must be stored somewhere.

c. An execution mode generator for generating an execution mode signal for controlling an execution mode of the array (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2). In regards to Wilkinson, the execution mode is dictated by the instruction to be processed by the elements.

d. A control circuit connected to each processing cell, each control circuit having inputs for receiving the row enable signal, the column enable signal, and the

execution mode signal, and including logic that outputs a first control signal for controlling input of the data to the operation unit of the cell, and a second control signal for controlling input of the context instruction to the context register of the cell (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2).

15. Referring to claim 8, Wilkinson has taught wherein the execution mode of the array includes:

a. A SIMD mode in which each enabled cell repeatedly executes on an updated context instruction (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2);

b. A programming mode in which an plurality of updated contexts are broadcast to the enabled cells, and the function of each cell is not updated (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2); and

c. A SIMD mode in which the context registers are frozen and each cell executes on its present context (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column

15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2); and

16. Referring to claim 9, Wilkinson has taught a method, comprising:

a. Enabling a sub-unit of cells for a new context instruction in an MxN array of cells, wherein each non-enabled cell maintains its present context instruction (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2); and

b. Providing the new context instruction to each cell in the sub-unit (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2).

17. Referring to claim 10, Wilkinson has taught wherein each masked cell keeps its internal states and the present context (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2).

18. Referring to claim 11, Wilkinson has taught a method of programming a operations context for a MxN array of cells, comprising:

a. Selecting an execution mode for each cell in the array, wherein the execution mode includes a MIMD execution mode and a SIMD execution mode (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13,

lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2);

b. Executing, by each cell having the MIMD execution mode, a present context (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2); and

c. Executing, by each cell having the SIMD execution mode, an updated context (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2).

19. Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilkinson et al., U.S. Patent Number 5,282,894 (herein referred to as Wilkinson) in view of Holsztynski, U.S. Patent Number 4,739,474 (herein referred to as Holsztynski).

22. Referring to claim 12, Wilkinson has taught a dynamically reconfigurable processing cell for an MxN array of cells (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2), comprising:

a. At least one functional unit configured to execute an operation (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2);

b. A context register, connected to each functional unit, configured to output a context instruction that controls each functional unit (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2). In regards to Wilkinson, the memory which provides the context, or instruction, to be executed functions the same as the context register.

c. A register file for storing a result from said at least one functional unit (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2);

d. A first control input connected to the register file for receiving a first enable signal that controls latching of the result from said at least one functional unit by the register file (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18

and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2); and

e. A second control input connected to the context register for receiving a second enable signal that controls latching of a next context instruction by the context register (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2).

23. Wilkinson has not taught a clock signal input for receiving a global clock signal. Holsztynski has taught a clock signal input for receiving a global clock signal (Holsztynski column 4, lines 23-24). A person of ordinary skill in the art at the time the invention was made, and as taught by Holsztynski, a clock signal input is needed to ensure the desired operations are performed on a data matrix, thereby ensuring the correct results are obtained and data coherency is maintained. Therefore, it would have been obvious at the time the invention was made to incorporate the clock signal input of Holsztynski in the device of Wilkinson to ensure correct results are obtained an data coherency is maintained.

24. Referring to claim 13, Wilkinson has taught wherein the first enable signal is configured to activate the plurality of sequential processing elements (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2).

25. Referring to claim 14, Wilkinson has taught wherein the second enable signal is configured to activate the context register, wherein the context register is adapted to receive a new context instruction only in the active state (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2). In regards to Wilkinson, the memory which provides the context, or instruction, to be executed functions the same as the context register.

26. Referring to claim 15, Wilkinson has taught wherein the first and second inputs are responsive to an enable signal provided by an external enable register (Wilkinson Abstract; column 8, lines 52-57; column 12, lines 7-18 and 48-58; column 13, lines 1-4 and 14-62; column 14, lines 22-50; column 15, lines 52-56; column 16, lines 7-64; column 17, line 28 to column 18, line13; Figure 1; and Figure 2). In regards to Wilkinson, the enable register is inherent since the signals which indicate which processing elements are not dozing must be stored somewhere.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Pechanek et al., U.S. Patent Number 6,128,720, has taught an array processor for SIMD and MIMD processes.

b. Huang, U.S. Patent Number 4,943,909, has taught an array processor for SIMD operations.

c. Taylor, U.S. Patent Number 4,992,933, has taught an array processor for SIMD operations with a controller.

d. Burnett, U.S. Patent Number 5,708,9\835, has taught an array processor for SIMD operations with a controller and memory.

e. Wilkinson et al., U.S. Patent Numbers 5,805,915 and 5,815,723, have taught n array processor for SIMD and MIMD operations with controllers and memories.

f. Rosen et al., U.S. Patent Number 5,832,291, has taught an array processor for SIMD operations with a controller.

g. Barker, U.S. Patent Number 5,717,943, has taught an array processor for SIMD operations with a controller.

h. Collins, U.S. Patent Number 5,963,745, has taught an array processor for SIMD operations with a controller.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
May 6, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100